Basic Study of Pulse Width Modulation System for Medium-Voltage High-Frequency Inverters

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Keywords Multi-level, High-frequency, Pulse pattern, Harmonic current

Abstract

Medium-voltage inverters for medium-voltage motor driving, as inverters of the multistage series cell system have been developed. The Pulse Width Modulation (PWM) system adopted for these inverters is generally an asynchronous PWM system. In the asynchronous PWM system, however, it is difficult to generate the command voltage output properly during a single period of the fundamental wave when the number of pulses are small. As a result of an increase in output frequency, various difficulties appear such that surge voltage is raised at motor terminals, harmonic current is increased, and low-frequency ripples are caused. These difficulties can, however, be removed by the use of a fixed pulse pattern system. When the fixed pulse pattern system is adopted, low-distortion pulse patterns are introduced beforehand and tabulated so that the output can be generated in synchronization with the voltage phase. We made a simulation to compare the features of the asynchronous PWM system with that of the fixed pulse pattern. As a result, we verified the validity of the latter system.

1 Preface

For medium-voltage motor driving that is applied to large-scale fans and pumps, direct-drive medium-voltage inverters are used because medium voltages can be directly generated. For this type of inverter, we developed the multistage series cell system inverter[1][2] where single-phase inverters are connected in a series.

The multistage series cell system inverters are operated in a multilevel driving mode. In this case, however, surge voltage may be raised at the motor terminal if there is a level skip (simultaneous change across two or more levels). It is, therefore, preferable to keep the voltage level variation in a step-by-step mode for the prevention of insulation breakdown. In regards to the control of the multistage series cell system inverters, the practical pulse modulation system[3][4] has been explored and studied by the market.

High output frequencies have recently been in demand for inverters and some challenges that cannot be solved by conventional control systems have occurred. In the conventional method, an asynchronous Pulse Width Modulation (PWM) system has been adopted in the case of pulse modulation for the multistage series cell system inverters. In the asynchronous PWM, the carrier frequency is set so that the gradient of triangle wave carrier is greater than that of the command voltage. When such a setting is made, the output voltage level does not cause a level skip and the motor surge voltage can be suppressed. If this setup criterion is used for high output frequencies, however, the carrier is pressed to rise to a higher frequency. If the carrier frequency is raised, switching loss is increased and this leads to the expansion of equipment size. If, however, the carrier frequency is kept low to control the high output frequency, the following three problems arise:

(1) Level skip is caused in the voltage level and the motor surge voltage is raised.

(2) The number of pulses is decreased in a single period of the fundamental wave and harmonic current is increased.

(3) As a result of asynchronization between the triangular wave carrier and output voltage, ripples become eminent in low frequencies below the fundamental wave frequency.

In order to control high output frequencies, therefore, an adequate modulation system is required, by which switching frequencies can be

kept low and three essential factors of motor surge voltage, harmonic current, and low-frequency current ripples can be suppressed.

This paper introduces the fixed pulse pattern system as a solution to these challenges. By virtue of the fixed pulse pattern system, low-distortion pulse patterns are introduced in advance and tabulated so that the output can be generated in synchronization with the voltage phase. For the confirmation of the resultant effect, we made a simulation level comparison between the fixed pulse pattern system and the asynchronous PWM system.

2 Circuit Configuration

Fig. 1 shows the circuit configuration of the multistage series cell system inverters. The three-phase input voltage is applied to each cell unit (U1, U2, ⋯, U6, V1, ⋯,V6, W1, ⋯, W6) through a multiple winding transformer. The cell unit is composed of a three-phase rectifier and a single-phase inverter, from which a single-phase AC voltage output is generated. The cell units in the respective phases are connected in series and the phase voltage added with cell unit outputs is applied to the motor. Since output at level −6 to level +6 in each phase can be generated in a 6-series configuration shown in **Fig. 1**, the phase voltage V_U can be operated at 13-level, the highest.

3 Pulse Modulation System

3.1 Asynchronous PWM System

Fig. 2 shows a control block diagram of the asynchronous PWM system. For an angular frequency command ω^*, stabilization correction of motor vibration is carried out with the use of the detected current in order to obtain a corrected angular frequency command ω^{**} and an Axis dq voltage command v_{dq}^*. By virtue of V/f control, both ω^{**} and v_{dq}^* are maintained at a constant ratio. By making integration of ω^{**} to attain the control phase θ, a three-phase voltage command v* is obtained through a process of dq/UVW transformation. In the PWM, a comparison is made between v* and the frequency-preset triangular wave carrier independent of ω^{**} so that the gate signal g can be defined based on the magnitude relationship.

Fig. 3 shows a comparison of carriers for the Phase Shift (PS) system. The asynchronous PWM system introduced in this paper is a PS system where a comparison is made with a carrier the phase of which is shifted. For simplification, a case

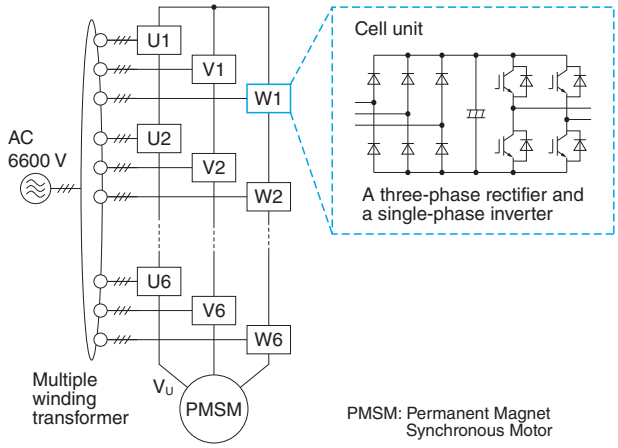


Fig. 1 Circuit Configuration of the Multistage Series Cell System Inverters

An inverter circuit configuration is shown, where six cells are connected in series in each phase.

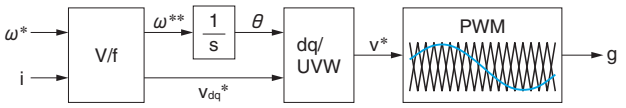


Fig. 2 Control Block Diagram of Asynchronous PWM System

The V/f control is performed for motor stabilization based on the detected current i.

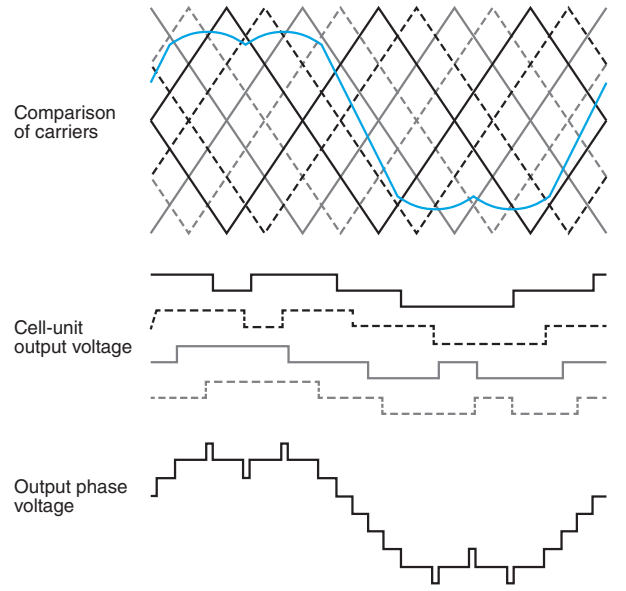


Fig. 3 Comparison of Carriers for the PS System

For multiple triangular wave carriers the phases of which are shifted at the same intervals, comparison is performed with the command voltage. Based on the result of comparison with each carrier, a cell unit voltage is obtained. The phase voltage is obtained by summing up all of the cell-unit voltages.

of four-series configuration is shown. A pair of a single carrier and another carrier reversed upside down is used to define an output voltage for each cell unit. The total sum of cell unit outputs functions as an output phase voltage. When this PS system is adopted, there can theoretically be a difficulty, such that a line voltage may cause a level skip. As such, this difficulty is cleared by the use of the Carrier Phase Selection (CPS) system[3] where an optimal carrier is selected by observing command voltage changes.

In the CPS system, the conditions for the prevention of a level skip in line voltage are given by Expression (1) below. Expression (1) provides a condition that the gradient of a carrier becomes greater than that of the command voltage. Value f_c is a carrier frequency (Hz) per cell unit, Value f_r is a command voltage frequency (Hz), and Value K is a modulation rate (0～1) based on common mode voltage PWM.

$$f_c = \frac{\sqrt{3}}{2} \pi \cdot f_r \cdot K \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

Expression (1) suggests that the carrier frequency f_c should be raised when f_r is high, more specifically: the output frequency is high.

In the asynchronous PWM system, the carrier frequency and the fundamental wave frequency are determined independently of each other. Consequently, according to a fundamental wave frequency, the number of pulses for a single period of the fundamental wave can change at multiple period intervals. In such a case, ripples at a frequency lower than that of the fundamental wave can occur according to the frequency of pulse number variation.

3.2 Fixed Pulse Pattern System

Fig. 4 shows a control block diagram of the fixed pulse pattern system. The process of V/f control and ω^{**} integration is the same as that of the asynchronous PWM system in Fig. 2. The only difference is that the output is a modulation rate command d. After V/f control, dq/UVW transformation is not performed. A reference table is picked up from the modulation rate command d and the gate signal g is generated from the table of the control phase θ. The respective table values are calculated in advance based on the derivations of pulse patterns as described in Section 4.

Fig. 5 shows the table comparison flowchart. According to this flowchart, a required reference table T is determined from the modulation rate command d and the output level L is defined by comparing T with the control phase θ. Based on the circuit configuration in Fig. 1, the gate signal g is defined to generate an output at L. By a series of these processes, a tabulated pulse pattern output can be generated according to the voltage phase. In this case, L denotes a phase voltage level after the multiplication of cell unit outputs. (Equivalent to V_U in Fig. 1) Regarding this table, tables of the respective

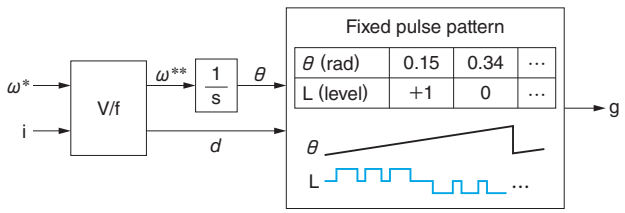


Fig. 4 Control Block Diagram of the Fixed Pulse Pattern System

Similarly as for Fig. 2, V/f control is performed here. A different point is that the input signal for modulation system is the modulation rate command d.

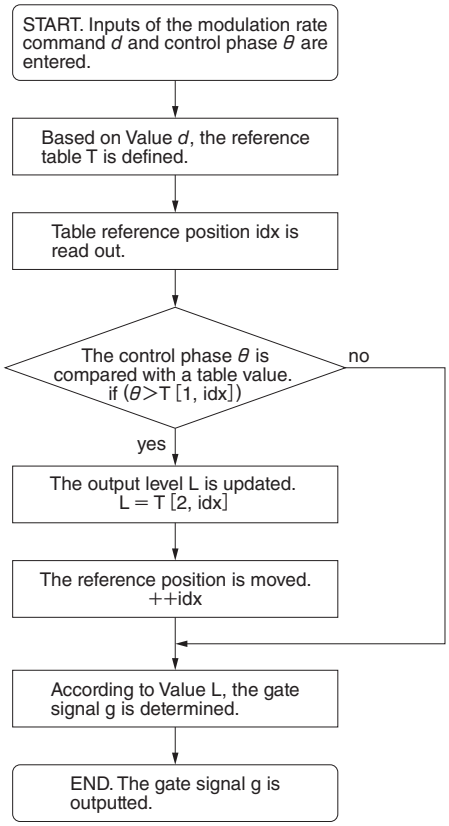


Fig. 5 Table Comparison Flowchart

The gate signal generation procedure is shown for the introduced system (fixed pulse pattern system). Based on the comparison between θ and table values, a required pulse pattern output is generated according to the table.

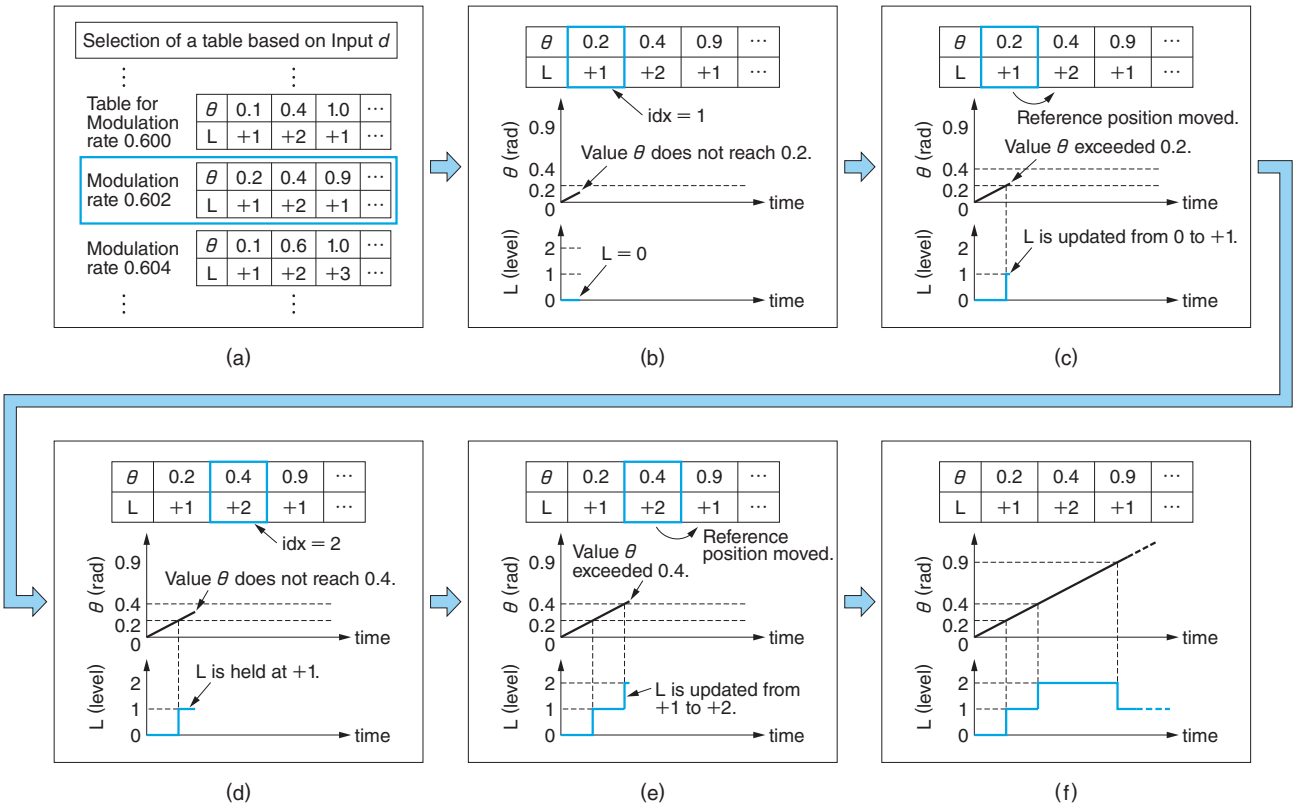


Fig. 6 **Operation of Table Comparison**

The operation flowchart in **Fig. 5** is explained in diagrams. In response to an increase in the control phase (voltage phase), the output levels make changes indicated in the table.

pulse patterns are established at the intervals of 0.1% to several percent within the scope of applicable modulation rates and a table of the modulation rate closest to *d* is picked up from the established tables and used as T.

Fig. 6 shows the operation of a table comparison. It shows the operation in **Fig. 5**. In (a), the reference table T is determined from the modulation rate command *d*. After that, a series of operation for table comparison is shown. The initial value is set at idx = 1 and L = 0. The first line of Table T involves the pulse pattern data θ and the second line saves the level data L. In (b), data is held at L = 0 because Value θ is smaller than the table phase value 0.2 rad at idx = 1 in T. In (c), θ increases to be greater than 0.2 rad and L is updated to Level +1 that is the level value at idx = 1. After level updating, idx is incremented. In (d), θ is increased than in (c), but it is still below the phase value 0.4 rad at idx = 2. Accordingly, L is kept held at Level +1. In (e), θ has exceeded the phase value 0.4 rad at idx = 2 and L is updated to the level value at idx = 2. Similarly in (f), updating and holding are carried out. L indicates that outputs of pulse patterns are generated according to table design.

4 Derivation of Pulse Patterns

In the asynchronous PWM system, the triangular wave carrier is compared with the command voltage and the voltage pulse width is defined so that the command voltage output can be generated based on the single-period average of the triangular wave. The asynchronous PWM system is based on the period of triangular waves. If a single period of the fundamental wave of the output voltage is taken into consideration, optimal pulses cannot always be generated. Accordingly, when the carrier frequency becomes closer to the fundamental wave frequency and the number of pulses in a single period of the fundamental wave is decreased, the resolution of command voltage is deteriorated and distortion in the output voltage is increased.

In the case of the fixed pulse pattern system, the pulse pattern is optimized in advance, based on the single period of the fundamental wave. An output voltage with minimal distortion can then be generated even though the number of pulses is decreased in the single period of the fundamental wave. How a pulse pattern with minimal distortion is derived is explained below.

Fig. 7 shows an example of a pulse pattern. When periodicity to the fundamental wave and symmetry of sinusoidal fundamental wave are taken into consideration, a pulse pattern is the basis, if it is symmetrical at every 90° as shown in (a).

Distortion in the pulse pattern is then examined by making the Fourier series expansion. Pattern (a) can be decomposed into three-level symmetrical pulse patterns at the intervals of 90°. Patterns (b) to (e) are the result of decomposition. After decomposition, the Fourier series expansion of pulses is carried out, and the resultant values are then added.

After the Fourier series expansion of (b), Expression (5) is obtained, Expression (2), Expression (3), and Expression (4) have been established. In these expressions, a_0, a_n, and b_n are Fourier coefficients, N is the number of cell unit tiers, and $f_A(\theta)$ is (b) expressed in Fourier series. The voltage level is normalized at the maximum level.

$$a_0=\frac{1}{\pi N}\left\{\int_{-\pi}^{-\pi+A}0dt+\int_{-\pi+A}^{-A}-1dt+\int_{-A}^{A}0dt+\int_{A}^{\pi-A}1dt+\int_{\pi-A}^{\pi}0dt\right\}=0 \quad \cdots\cdots\cdots\cdots (2)$$

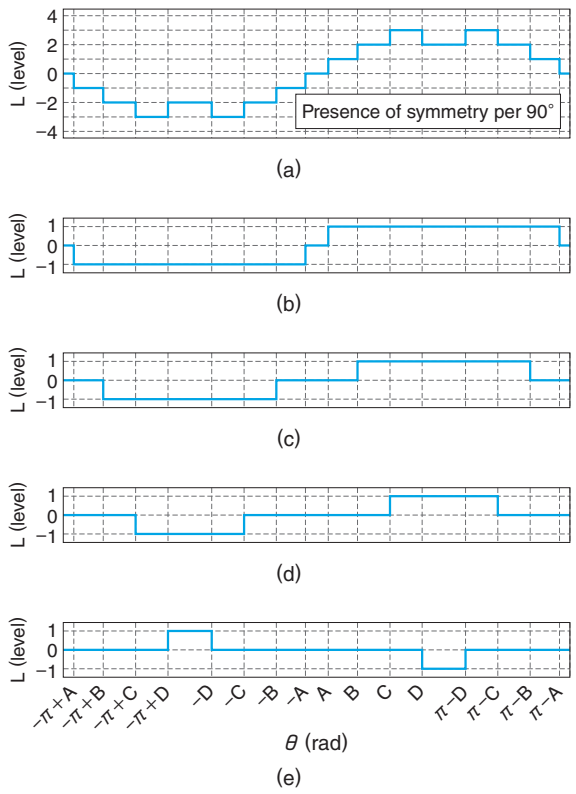


Fig. 7 Example of Pulse Pattern

Pulse patterns assuming the operation in Section 4 are shown. The result of decomposition of (a) is turned into (b) to (e).

$$a_n=\frac{1}{\pi N}\left\{\int_{-\pi}^{-\pi+A}0\cdot\cos(nt)dt+\int_{-\pi+A}^{-A}-1\cdot\cos(nt)dt+\int_{-A}^{A}0\cdot\cos(nt)dt+\int_{A}^{\pi-A}1\cdot\cos(nt)dt+\int_{\pi-A}^{\pi}0\cdot\cos(nt)dt\right\}$$
$$=0\ (n=1,\ 2,\ 3,\ 4,\ \cdots) \quad \cdots\cdots\cdots\cdots (3)$$

$$b_n=\frac{1}{\pi N}\left\{\int_{-\pi}^{-\pi+A}0\cdot\sin(nt)dt+\int_{-\pi+A}^{-A}-1\cdot\sin(nt)dt+\int_{-A}^{A}0\cdot\sin(nt)dt+\int_{A}^{\pi-A}1\cdot\sin(nt)dt+\int_{\pi-A}^{\pi}0\cdot\sin(nt)dt\right\}$$
$$=\begin{cases}\dfrac{4}{n\pi N}\cos(nA) & (n=1,\ 3,\ 5,\ 7,\ \cdots)\\ 0 & (n=2,\ 4,\ 6,\ 8,\ \cdots)\end{cases} \quad \cdots\cdots (4)$$

$$f_A(\theta)=\frac{a_0}{2}+\sum_{n=1}^{\infty}\{a_n\cos(n\theta)+b_n\sin(n\theta)\}$$
$$=\frac{4}{\pi N}\left\{\cos A\sin\theta+\frac{1}{3}\cos(3A)\sin(3\theta)+\frac{1}{5}\cos(5A)\sin(5\theta)+\cdots\right\} \quad \cdots\cdots\cdots\cdots (5)$$

Since Pattern (a) is based on the premise of sinusoidal symmetry, cosine components and even-order harmonic components are eliminated in Expression (5).

Similar calculation is performed for (c)～(e) and the respective figures are added together. As a result, an amplitude of the n-th harmonic voltage is obtained for the pulse pattern of (a), which is expressed H_n Expression (6). Since the level change of (e) is in the reverse direction of (b), (c), and (d), the term relating to D in Expression (6) is attached with a negative sign.

$$H_n=\left|\frac{4}{n\pi N}\{\cos(nA)+\cos(nB)+\cos(nC)-\cos(nD)\}\right| \quad (n=1,\ 3,\ 5,\ 7,\ \cdots) \quad \cdots\cdots (6)$$

Except for H_1 in the fundamental wave amplitude, all figures H_3, H_5, H_7, ⋯ are the distortion components in output voltage. The smaller the values of these H_3, H_5, H_7, ⋯, the smaller the distortion in the pulse pattern.

Even if other settings about the number of switching and the directions of level changes are used, the amplitude of the n-th harmonic voltage can be calculated based on the aforementioned calculation procedures. Now, Expression (6) is used to

examine the evaluation function for pulse pattern deriving operation. The evaluation function is based on an example of the report[5] in the past.

Firstly, Expression (7) must be kept to obtain the fundamental wave of voltage based on the modulation rate command d.

$$d=\frac{4}{\pi N}(\cos A+\cos B+\cos C-\cos D)\cdots\cdots(7)$$

It is then necessary to design the phases ($A\cdot B\cdot C\cdot D$) of the respective level changes in order not to cause a level skip. In this case, phase width θ_1 rad among level changes may be determined based on Expression (8). In this expression, Value t_{skip} is a maximum time width (s) simulatively regarded as a level skip and Value f_{out} is the fundamental wave frequency (Hz) at which a pulse pattern is used.

$$\theta_1>2\pi\cdot f_{out}\cdot t_{skip}\cdots\cdots(8)$$

In regard to harmonics, a standing goal is the reduction of harmonic currents. Insofar as a three-phase equilibrium of voltage is maintained, harmonic voltages in the order of multiples of 3 do not affect motor currents. For this reason, it is unnecessary to consider harmonic voltages in the order number of $n=3, 6, 9, \cdots$, and the order number $n=5, 7, 11, 13, \cdots$only may simply be taken into consideration. In addition, due to the effect of the inductance component of a motor, currents are minimally affected by harmonic voltages in higher orders. Accordingly, the reduction of harmonic voltages in lower orders is in higher preference. As a result, Expression (9) is regarded as a conditional formula for harmonic components. In Expression (9), the denominator of a coefficient is n^2 where inductance component is taken into consideration.

$$\left|\frac{4}{n^2\pi N}\{\cos(nA)+\cos(nB)+\cos(nC)-\cos(nD)\}\right| \quad (n=5,\ 7,\ 11,\ 13,\ 17,\ \cdots)\quad\cdots(9)$$

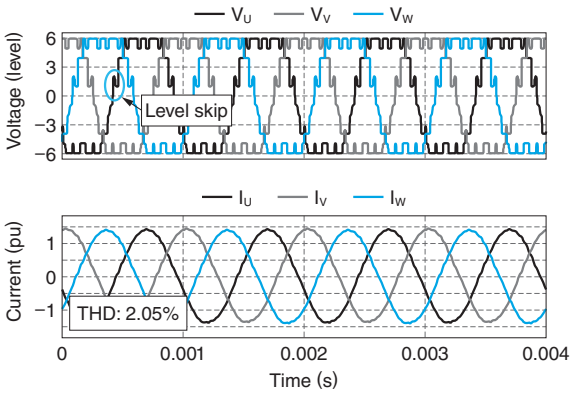
Based on Expression (7) and Expression (8), a favorable combination of Phases $A\cdot B\cdot C\cdot D$ is searched for in order to reduce the effect of Expression (9). After the combination of $A\cdot B\cdot C\cdot D$ has been obtained, the pulse pattern for a single period of the fundamental wave is defined based on the symmetry of the pulse patterns. In doing so, it is possible to derive a pulse pattern to minimize the harmonic current based on a single period of the fundamental wave, free from level skip in voltage.

5 Result of Simulation

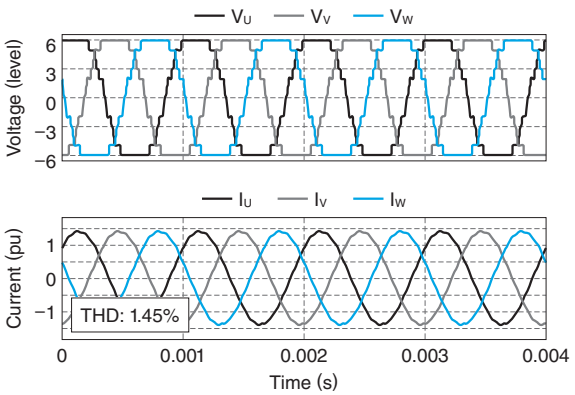
By comparing the result of the asynchronous PWM system, the effect of the fixed pulse pattern system is confirmed through simulation.

The carrier frequency of the asynchronous PWM system was fixed at 12,000 Hz throughout the equipment. This setting was made to establish a condition that the switching frequency is kept almost identical with that of the fixed pulse pattern system at the fundamental wave frequency 1000 Hz of the output voltage.

Fig. 8 shows the result of simulation at fundamental wave frequency 1000 Hz. The Total Harmonic Distortion (THD) is based on a result of the current analysis in Phase U. After attaining the result of Discrete Fourier Transformation (DFT) obtained at the intervals of 5 Hz, all components of frequencies higher than those of the fundamental wave were summed up. For voltage wave forms of the asynchronous PWM system in (a), the number of pulses



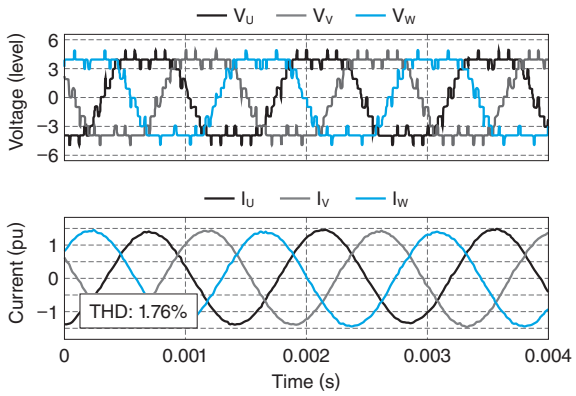
(a) Asynchronous PWM system



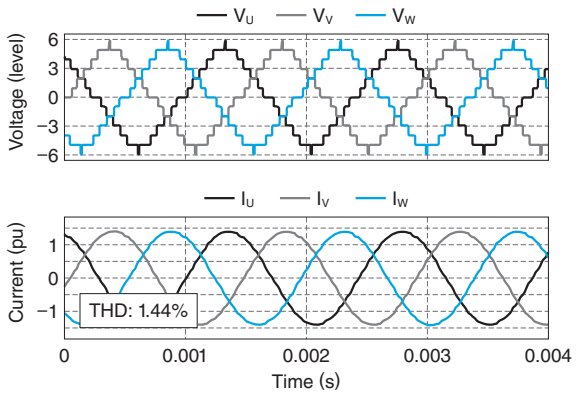
(b) Fixed pulse pattern system

Fig. 8 **Result of Simulation at Fundamental Wave Frequency 1000 Hz**

The effect of the introduced system is shown. In (b), THD is small and there is no level skip in voltage.



(a) Asynchronous PWM system



(b) Fixed pulse pattern system

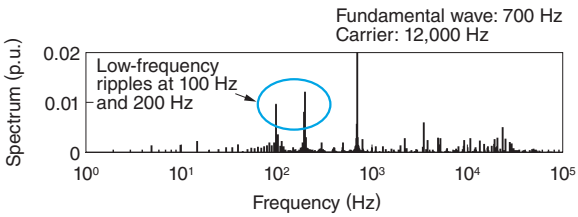
Fig. 9 **Result of Simulation at Fundamental Wave Frequency 700 Hz**

The effect of the introduced system is examined here. THD is smaller in (b). In (a), the number of voltage pulses is influenced by a period and the peak value of current is increased by each period.

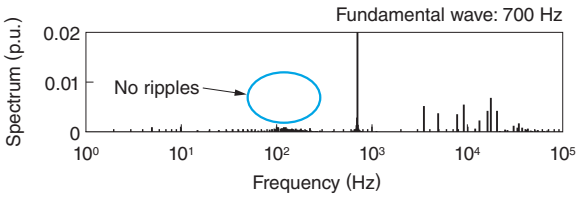
is decreased and asymmetrical patterns are attained in positive and negative domains. In (b), on the other hand, a symmetry is secured for the fixed pulse pattern system. By virtue of its influence, the current THD is kept smaller in (b).

When a maximum modulation rate is adopted, the setting of carrier frequency 12,000 Hz does not satisfy Equation (1) against the fundamental wave frequency 1000 Hz. According to this, for the voltage waveform in (a), a level skip at the voltage level is caused in the vicinity of the zero cross where the gradient of command voltage is large. Since level skip in the voltage waveform of (a) can cause an increase in the surge voltage of a motor, it is necessary to take adequate countermeasures by using a filter or the like. In (b), there are no level skips.

Fig. 9 shows the result of simulation at the fundamental wave frequency 700 Hz. The result shows



(a) Asynchronous PWM system



(b) Fixed pulse pattern system

Fig. 10 **Result of Phase U Current DFT at Fundamental Wave Frequency 700 Hz**

The result of analysis by discrete Fourier transformation on Phase U current I_U in **Fig. 8** is shown. Low-frequency current ripples fractionally seen in **Fig. 8** are clearly shown in a form of 100 Hz and 200 Hz spectra.

that the THD value is smaller in (b). The fundamental wave frequency 700 Hz is not an integral multiple of carrier frequency 12,000 Hz. In the asynchronous PWM system, the number of pulses in a single period of the fundamental wave varies at multiple periods. Examining the vicinity of positive peaks of V_U in (a), the number of pulses at the first and second peaks is different from that at the third. As a result of this phenomenon, the peak value of I_U in (a) becomes large for each period. The current of (a) involves ripples at frequencies lower than those of the fundamental wave.

Fig. 10 shows the result of Phase U current DFT at a fundamental wave frequency 700 Hz. The fundamental wave frequency component is normalized so that it becomes unity. Based on **Fig. 10**, the frequency component of the current is examined. According to the result for the asynchronous PWM system, the spectra can be observed at 100 Hz and 200 Hz; these are in a domain of low frequencies, lower than the fundamental wave frequency 700 Hz. The result of DFT also indicates that (a) involves low-frequency components. While in the fixed pulse pattern system, there is no presence of ripples in low-frequency zones. This is because the fixed pulse pattern system is based on the output voltage that is synchronized with the voltage phase of the fundamental wave.

6 Postscript

When designing the multistage series cell system inverters in order to cope with high frequencies, there arise three essential challenges in the case of the asynchronous PWM system: (1) an increase in motor surge voltage due to level skip in voltage, (2) an increase in harmonics in output current, and (3) an increase in low-frequency ripples. For solutions, we adopted the fixed pulse pattern system.

At the fundamental wave frequency 1000 Hz, the obtained result was that the current THD is smaller than the case of asynchronous PWM system. Even at the fundamental wave frequency 700 Hz, the current THD is also reduced and there is no presence of low-frequency ripples.

From now on, we will work on the operation verification of the fixed pulse pattern system through experiments.

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