Establishment of Electrostatic Discharge (ESD) Noise Analyzing Technology

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Abstract

As a result of a change to using low voltages and higher speeds of semiconductor devices, securing durability against electrostatic noises for electronic products is becoming more difficult.

Formerly, the required durability was secured by confirming the durability level by performing the Electrostatic Discharge (ESD) immunity test on actual products and taking measures and repeating the testing. This method, however, resulted in increased man-hours to take measures and has become a factor in the delay of process.

We have, therefore, established an electrostatic noise analysis technology for devices equipped with printed circuit boards using an electromagnetic field analysis tool.

Through such analytic approaches, it is possible to visualize an electromagnetic field distribution caused by application of ESD noise and examine its effect to specific signal lines.

As a result, it is possible to quantify the effects of ESD noise on devices and reduce rework.

It will, therefore, be possible to quickly introduce high-quality products with high noise immunity to the market.

1 Preface

In the winter season, everybody experiences an electric shock when touching the door of a car or a house. This is caused by an electrostatic discharge. Similarly, when one touches an electronic product or equipment, there can be a chance to cause an Electrostatic Discharge (ESD). The generated static electricity affects the inside of electronic devices as a static electricity noise, whereby causing malfunctions, stoppages, and failures. Malfunctions in electronic products can lead to failures of an entire system, and the impact can be enormous.

To investigate the presence of such a defect caused by ESD noise, we use a tester to cause an ESD to examine the durability by applying ESD noise to electronic equipment. If the durability is found insufficient due to testing, it is necessary to take an adequate measure. If the result of taking measures is considered unsatisfactory, the testing needs to be repeated. In some cases, a many man-hours may be required. Accordingly, countermeasures against ESD noise must be taken efficiently during the limited period of the development stage.

Consequently, we established an ESD noise analytic technology to reduce the development period by using an electromagnetic field analytical tool. This paper introduces the ESD noise analytic technology.

2 ESD Noise Analytic Technology

2.1 Modeling Technology

The accuracy of analytical results and analyzing times are a tradeoff. If the environment of actual machine testing is fully put into modeling, the analyzing time is increased. Accordingly, modeling is carried out to grasp the influence of the ESD noise while proper simplification is conducted.

(1) Casing model (see Fig. 1.)

Modeling of overall casing is carried out based on the design data of a three-dimensional CAD.

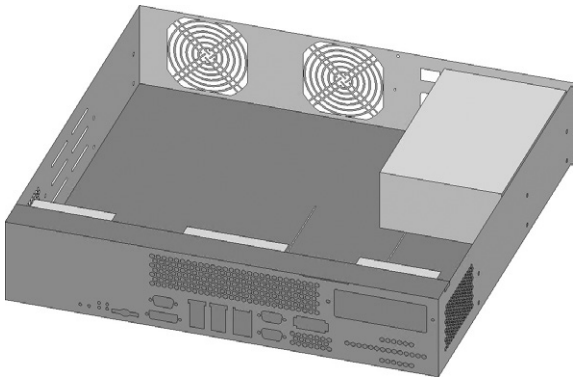

Fig. 1 Casing Model

A casing model acquired from three-dimensional CAD is shown.

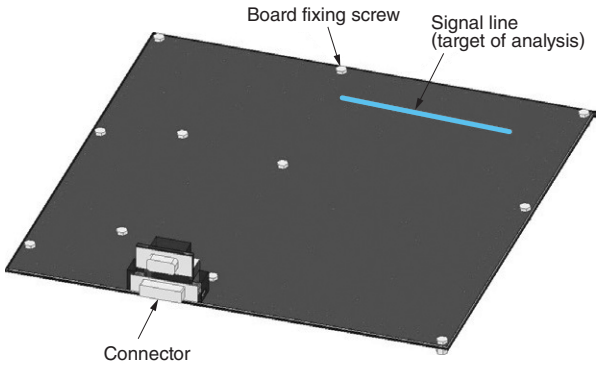

Fig. 2 Printed Circuit Board Model

A printed circuit board model acquired from three-dimensional CAD is shown.

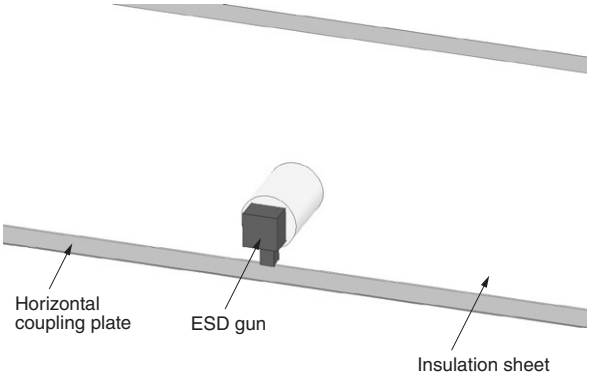

Fig. 3 Analytical Environment Model

A model of analytical environment established in reference to the actual machine testing environment is shown. (A horizontal coupling plate, insulation sheet, and ESD gun are modeled.)

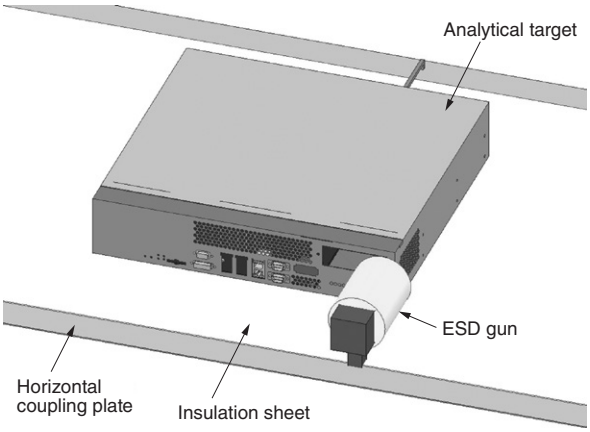

Fig. 4 Analytical Model

A model is shown, which is a combination of the respective models in Fig. 1, Fig. 2, and Fig. 3. Using this model, ESD noise analysis is carried out.

Casing modeling of the electric discharge course between metallic parts caused by the ESD is conducted.

(2) Printed circuit board model (see Fig. 2.)

Based on the design data of the Printed Circuit Board (PCB) CAD, PCB modeling is carried out by extracting the parts (mainly connectors and board fixing screws) that can be target signals for analysis and a route of the ESD.

(3) Analytical environment model (see Fig. 3.)

Analytical environment modeling of an ESD gun and for actual testing environments is established. Conforming to the testing conditions, an ambient environment is set up. If the testing environment is totally completely put into modeling, however, the analyzing space is expanded and analyzing time may be extended. For this reason, only part of the environment was modeled.

2.2 ESD Noise Analysis

Within the electromagnetic field analytic tool called “Ansys HFSS”, analysis is carried out on a model set up by the method described in **Section 2.1** above. Fig. 4 shows an analytical model. A required voltage is set up and applied to the analytical target. For the result of analysis, electromagnetic field distribution and voltage are checked.

(1) Analysis of electromagnetic field distribution

It is possible to analyze a current distribution on the unit surface and an electromagnetic field generated within the unit. Fig. 5 shows the current density distribution of a unit. According to the level of current density, a current flowing route can be surmised when an electrostatic discharge is applied to the casing.

(2) Voltage analysis

Voltages of the target device and wirings can be output in waveforms on the time axis. Fig. 6 shows voltage waveforms by two designs (Design A

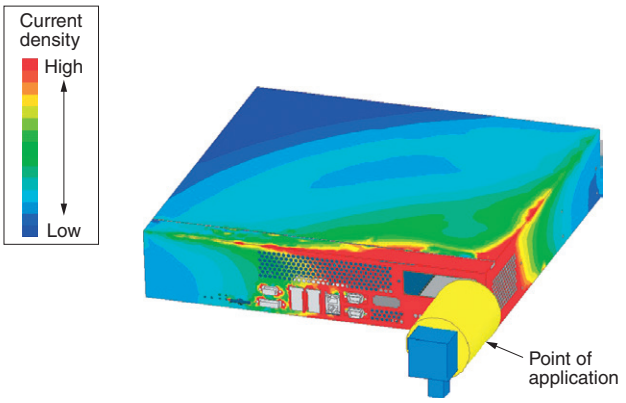

Fig. 5 Current Density Distribution of Unit

Current density distribution of a unit surface is shown. It is possible to examine how the current is spread over according to the timing.

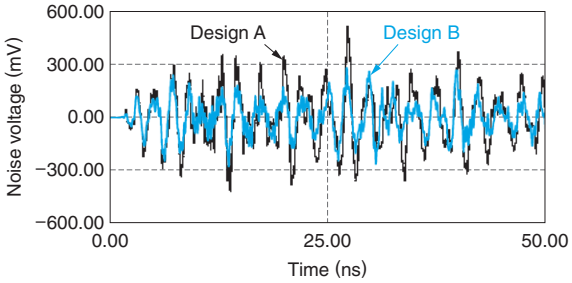

Fig. 6 Voltage Waveforms in Specific Wiring

Voltage waveforms of two designs (Design A and Design B) are shown.

and Design B). For Design A, parts not prepared for countermeasures against ESD noise are mounted. For Design B, parts prepared for countermeasures against ESD noise are mounted. When these two designs are compared with each other, the peak value of voltage applied to the target is lowered and influence is reduced in the case of Design B.

In this manner, it is possible to utilize the result to determine the casing structure and board layout based on this result where electromagnetic field distribution is visually understandable. In addition, a quantitative result can be used to identify the adequacy of countermeasures through the analysis of currents and voltages in a specific device and signal lines.

3 Postscript

This paper introduced the ESD noise analysis technology that we are working on. The acquisition of electromagnetic field distribution, current and voltage, and visual identification of potential problem areas enable countermeasures to be taken in advance. In order to utilize it at the design stage of development, however, it is necessary to evaluate the obtained analysis results and link them to efficient countermeasures.

In the future, we will work to establish quantitative evaluation methods and judgment criteria for analysis results so that countermeasures can be taken at the design stage of development.